What is claimed is:

1. A method for evaluating a shorting defect in an integrated circuit, said method comprising:

reading a plurality of quiescent power-plane current values at a plurality of corresponding power-plane voltages for a test vector for which said shorting defect is activated;

detecting a change in linearity of said plurality of power-plane current values with respect to said power-plane voltages; and

evaluating a severity of said shorting defect in conformity with a result of said detecting.

2. The method of Claim 1, further comprising determining a range of power-plane voltages above which said detecting detects that said plurality of power-plane current values are linear with respect to said power plane voltages, and wherein said evaluating evaluates said severity in conformity with said range.

3. The method of Claim 2, further comprising:

computing a first derivative of said quiescent power-plane current values at multiple ones of said power-plane voltages; and

detecting a peak value of said computed first derivative, and wherein said determining determines a lower bound of said range as a voltage corresponding to said peak value.

4. The method of Claim 1, further comprising:

second reading a second plurality of quiescent power-plane current values at said plurality of power-plane voltages for a second test vector for which said shorting defect is not activated; and

subtracting said second plurality of quiescent power-plane current values from said plurality of quiescent power-plane current values read by said reading, whereby said plurality of quiescent power-plane current values are normalized, and wherein said detecting is performed on said normalized quiescent power-plane current values.

5. The method of Claim 4, further comprising selecting a second test vector as a vector having a lowest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.

6. The method of Claim 1, wherein said evaluating comprises:

determining whether or not a power-plane voltage corresponding to said change in linearity is above a predetermined threshold; and

in response to determining that voltage is above said predetermined threshold, rejecting said integrated circuit as a failure.

7. The method of Claim 1, further comprising selecting said test vector as a vector having a highest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.

8. A computer program product for use with a workstation computer, wherein said computer program product comprises signal bearing media containing program instructions for execution within said workstation computer for evaluating a shorting defect in an integrated circuit, wherein said program instructions comprise program instructions for:

reading a plurality of quiescent power-plane current values at a plurality of corresponding power-plane voltages for a test vector for which said shorting defect is activated;

detecting a change in linearity of said plurality of power-plane current values with respect to said power-plane voltages; and

evaluating a severity of said shorting defect in conformity with a result of said detecting.

9. The computer program product of Claim 8, wherein said program instructions further comprise program instructions for determining a range of power-plane voltages above which said program instructions for detecting detect that said plurality of power-plane current values are linear with respect to said power plane voltages, and wherein said program instructions for evaluating evaluate said severity in conformity with said range.

10. The computer program product of Claim 9, wherein said program instructions further comprise program instructions for:

computing a first derivative of said quiescent power-plane current values at multiple ones of said power-plane voltages; and

detecting a peak value of said computed first derivative, and wherein said program instructions for determining determine a lower bound of said range as a voltage corresponding to said peak value.

11. The computer program product of Claim 8, wherein said program instructions further comprise program instructions for:

second reading a second plurality of quiescent power-plane current values at said plurality of power-plane voltages for a second test vector for which said shorting defect is not activated; and

subtracting said second plurality of quiescent power-plane current values from said plurality of quiescent power-plane current values read by said reading, whereby said plurality of quiescent power-plane current values are normalized, and wherein said program instructions for detecting operate on said normalized quiescent power-plane current values.

12. The computer program product of Claim 11, wherein said program instructions further comprise program instructions for selecting a second test vector as a vector having a lowest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.

13. The computer program product of Claim 8, wherein said program instructions for evaluating comprise program instructions for:

determining whether or not a power-plane voltage corresponding to said change in linearity is above a predetermined threshold; and

in response to determining that voltage is above said predetermined threshold, rejecting said integrated circuit as a failure.

14. The computer program product of Claim 8, wherein said program instructions further comprise program instructions for selecting said test vector as a vector having a highest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.

15. A workstation comprising:

a memory for storing program instructions and data values for evaluating a shorting defect in an integrated circuit;

a processor for executing said program instructions, wherein said program instructions comprise program instructions for:

reading a plurality of quiescent power-plane current values at a plurality of corresponding power-plane voltages for a test vector for which said shorting defect is activated;

detecting a change in linearity of said plurality of power-plane current values with respect to said power-plane voltages; and

evaluating a severity of said shorting defect in conformity with a result of said detecting.

16. The workstation of Claim 15, wherein said program instructions further comprise program instructions for determining a range of power-plane voltages above which said program instructions for detecting detect that said plurality of power-plane current values are linear with respect to said power plane voltages, and wherein said program instructions for evaluating evaluate said severity in conformity with said range.

17. The workstation of Claim 16, wherein said program instructions further comprise program instructions for:

computing a first derivative of said quiescent power-plane current values at multiple ones of said power-plane voltages; and

detecting a peak value of said computed first derivative, and wherein said program instructions for determining determine a lower bound of said range as a voltage corresponding to said peak value.

18. The workstation of Claim 15, wherein said program instructions further comprise program instructions for:

second reading a second plurality of quiescent power-plane current values at said plurality of power-plane voltages for a second test vector for which said shorting defect is not activated; and

subtracting said second plurality of quiescent power-plane current values from said plurality of quiescent power-plane current values read by said reading, whereby said plurality of quiescent power-plane current values are normalized, and wherein said program instructions for detecting operate on said normalized quiescent power-plane current values.

19. The workstation of Claim 18, wherein said program instructions further comprise program instructions for selecting a second test vector as a vector having a lowest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.

20. The workstation of Claim 15, wherein said program instructions for evaluating comprise program instructions for:

determining whether or not a power-plane voltage corresponding to said change in linearity is above a predetermined threshold; and

in response to determining that voltage is above said predetermined threshold, rejecting said integrated circuit as a failure.

21. The workstation of Claim 15, wherein said program instructions further comprise program instructions for selecting said test vector as a vector having a highest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.